

ECE 340 Download AND-OR Circuit to Basys FPGA Board

Introduction

In this exercise, you will download the AND_OR module (shown in Figure 1 below) that you completed in the previous two lab exercises. You have already created a test bench and simulated this circuit. Now, pins will be assigned to switches and lights on the Basys FPGA Board, and the circuit will be programmed into the FPGA, to allow testing of the actual hardware.

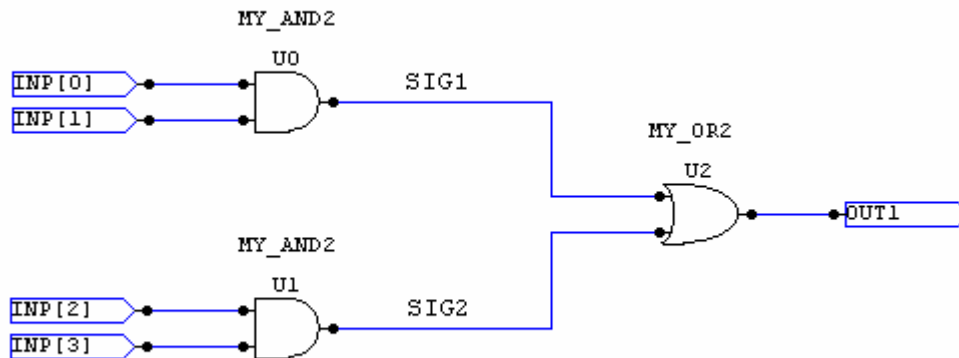


Figure 1: Schematic for Upper-Level Test Bench with AND_OR as UUT

Note: The *Diligent Basys Board Reference Manual*, the *Basys Basic Systemes Board Schematic Diagram*, and the *ISE 8.2i Quick Start Tutorial* will be useful during this exercise. Download them from <http://emp.byui.edu/fisherr/Tools.htm> or from our Blackboard course page under *Software, and References*.

Objectives

After completing this lab, you will be able to:

- Assign FPGA pins to input switches and output displays on the Basys board.
- Download a design into the Basys FPGA Board.
- Test an FPGA circuit for correct operation.

Procedure

1. Start the ISE Navigator. See the *ISE 8.2i Quick Start Tutorial*.
2. Open the previous project and update the FPGA information.

Select *File* → *Open Project*

Navigate to *C:\Xilinx\Labs\Lab3* and select *Lab3.isc*.

The screenshot shows the Xilinx ISE Design Summary window for a project named 'Lab3'. The window is divided into several panes:

- Sources for: Synthesis/Implementation:** Shows a tree view of the project files, including 'AND_OR (AND_OR.v)' and its sub-modules 'U0 - MY_AND2 (MY_AND2.v)', 'U1 - MY_AND2 (MY_AND2.v)', and 'U2 - MY_OR2 (MY_OR2.v)'.
- FPGA Design Summary:** A tree view of the design summary contents, including 'Summary', 'IOB Properties', 'Timing Constraints', 'Pinout Report', 'Clock Report', 'Errors and Warnings', 'Synthesis Messages', 'Translation Messages', 'Map Messages', 'Place and Route Messages', 'Timing Messages', 'Elgen Messages', 'All Current Messages', and 'Detailed Reports'.
- LAB3 Project Status:** A table showing project details:

Property	Value	Current State	Notes
Project File:	Lab3.isc	Programming File Generated	
Module Name:	AND_OR	• Errors:	No Errors
Target Device:	xc3s100e-5vq100	• Warnings:	No Warnings
Product Version:	ISE, 8.1i	• Updated:	Wed Nov 8 01:06:23 2006
- Device Utilization Summary:** A table showing logic utilization:

Logic Utilization	Used	Available	Utilization	Notes
Number of 4 input LUTs	1	1,920	1%	
Logic Distribution				
Number of occupied Slices	1	960	1%	
Number of Slices containing only related logic	1	1	100%	
Number of Slices containing unrelated logic	0	1	0%	
Total Number of 4 input LUTs	1	1,920	1%	
Number of bonded IOBs	5	66	7%	
Total equivalent gate count for design	6			
Additional JTAG gate count for IOBs	240			
- Performance Summary:** A table showing timing and pinout data:

Property	Value	Pinout Data	Pinout Report
Final Timing Score:	0		Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints		
- Detailed Reports:** A table showing the status of generated reports:

Report Name	Status	Generated	Errors	Warnings	Infos

Double click on the FPGA in the *Sources* window.

Enter the values shown above in the *Device Properties* box and click *OK*.

The screenshot shows the 'Project Properties' dialog box in Xilinx ISE. The dialog box has a table of properties and values, and several checkboxes at the bottom.

Property Name	Value
Product Category	All
Family	Spartan3E
Device	XC3S100E
Package	VQ100
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary	<input checked="" type="checkbox"/>
Enable Message Filtering	<input type="checkbox"/>
Display Incremental Messages	<input type="checkbox"/>

Buttons: OK, Cancel, Default, Help

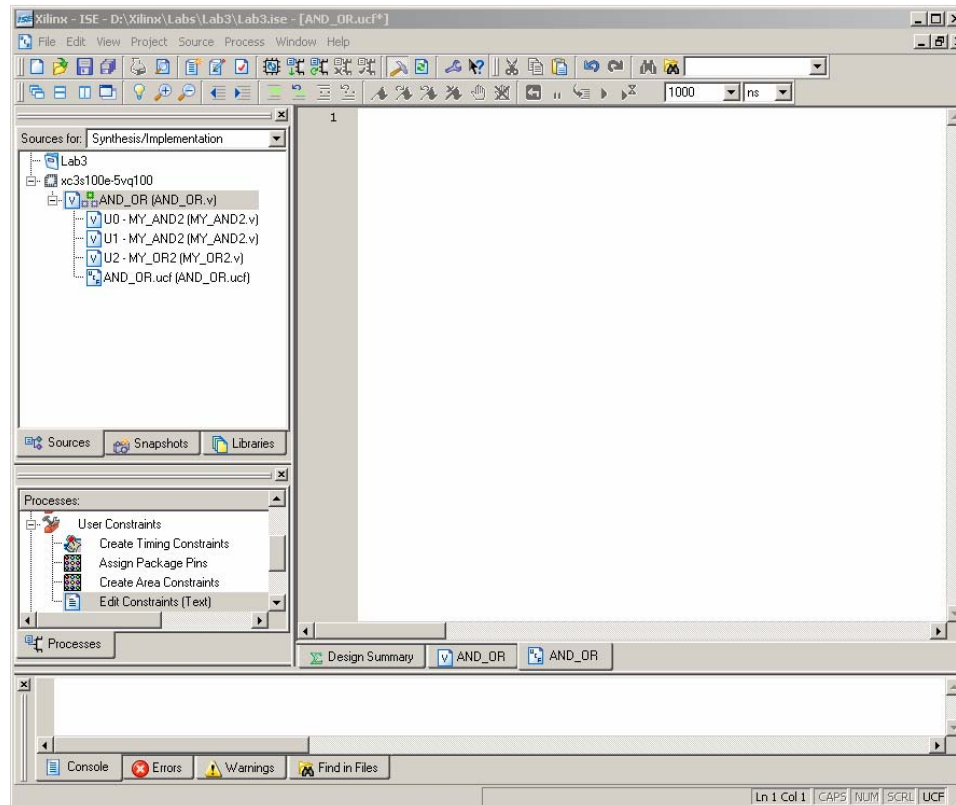
Click on the top level module (AND_OR.v).

3. Assign package pins.

Select AND_OR.v as the source file in the *Sources* window. Then expand *User Constraints* in the *Processes* window.

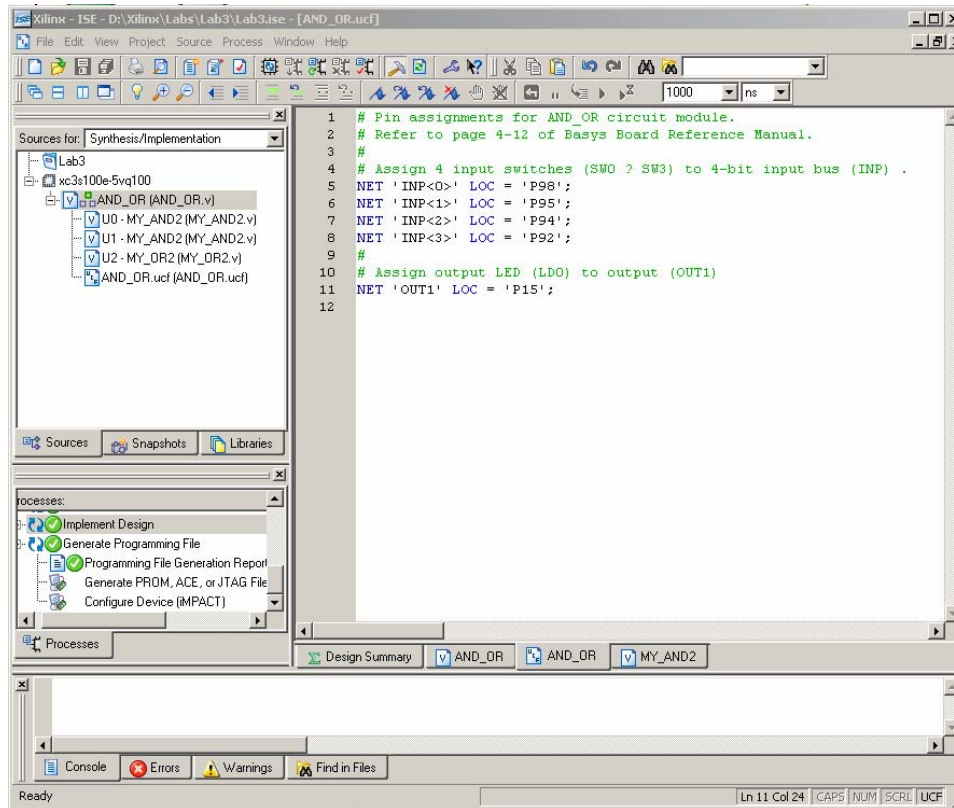
Double click *Constraints (Text)*.

A dialog box will open that asks to add an Implementation Constraint File (UCF) to the project. Click Yes. An editing window will appear.



Type the following code, starting with line 1, as shown in the figure below.

```
# Pin assignments for AND_OR circuit module.  
# Refer to page 4-12 of Basys Board Reference Manual.  
#  
# Assign 4 input switches (SW0 – SW3) to 4-bit input bus (INP) .  
NET 'INP<0>' LOC = 'P98';  
NET 'INP<1>' LOC = 'P95';  
NET 'INP<2>' LOC = 'P94';  
NET 'INP<3>' LOC = 'P92';  
#  
# Assign output LED (LD0) to output (OUT1)  
NET 'OUT1' LOC = 'P15';
```



Save the Implementation Constraint File (UCF).

- Download the circuit into the FPGA and test its operation.

Make sure the JTAG3 cable and the power supply are connected to the Basys Board.

Move the jumper on JP2 from the ROM position to the JTAG position. This will cause the FPGA to be programmed from the cable instead of reading the default program from the on-board ROM.

Double click on *Implement Design* in the *Processes* window. If there are no problems, a green check mark will replace the orange question mark.

Expand the *Generate Programming File* menu in the *Processes* window and double click *Configure Device (iMPACT)*. Wait for the new (iMPACT) window) to appear.

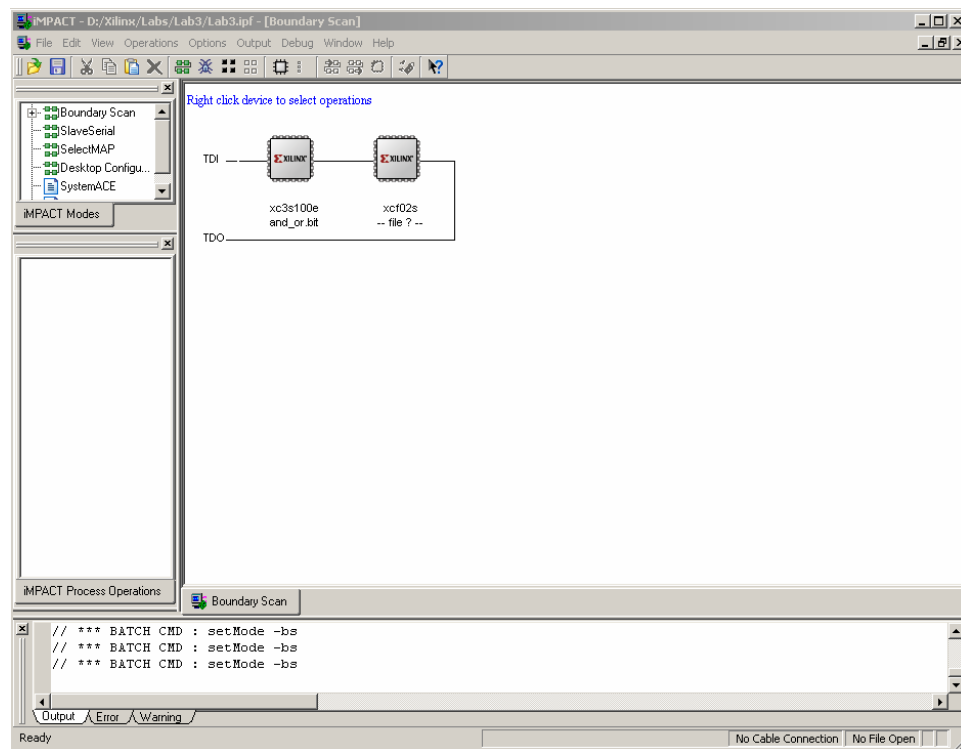
Select *Configure devices using Boundary scan (JTAG)* with the default option (*Automatically connect to a cable and identify Boundary-SCan chain*).

After the identification process is complete, a small window called *Assign a New Configuration File* will appear. Select *and_or.bit* (or other *.bit file if

you have named is differently). This is the file that will be programmed into the XC3S100E FPGA.

The same window will again appear. This time it is asking for the file to be programmed into the XCF02 Platform Flash ROM. Do not program the ROM. Select *Bypass* instead.

IMPORTANT: Why should you select *Bypass*? If you, instead, assign any file to this ROM, the default program & FPGA configuration will be erased. According to the ECE Department at the University of Minnesota, irreparable damage to your board will occur if your program has any errors. Do you want to risk it?



Right click on the *xc3s100e* device and select *Program*. Click *OK* to accept the default values in the *Programming Properties* window.

If all goes well, you will receive a message that states, "Programming Succeeded."

You may now remove the JTAG cable and test the hardware using the four input switches and the output LED.

NOTE: The bit stream you downloaded is volatile, which means that the FPGA is erased every time power is removed.