

ECE 340 Download AND-OR Circuit to Spartan 3E FPGA Board

Introduction

In this exercise, you will download the AND_OR module (shown in Figure 1 below) that you completed in the previous two lab exercises. You have already created a test bench and simulated this circuit. Now, pins will be assigned to switches and lights on the S3E FPGA Board, and the circuit will be programmed into the FPGA, to allow testing of the actual hardware.

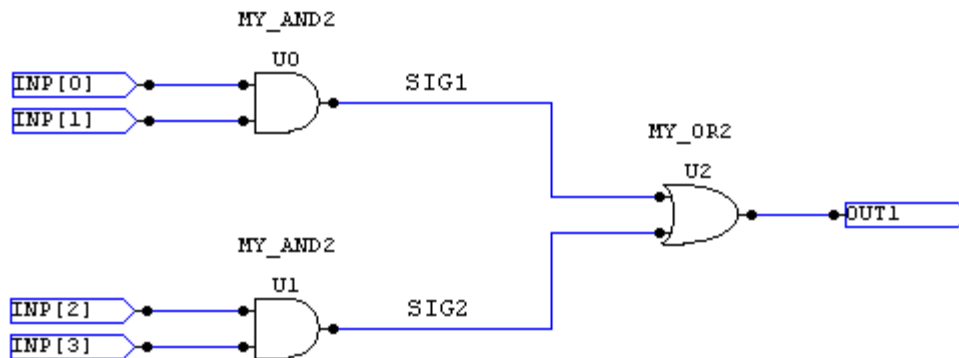


Figure 1: Schematic for Upper-Level Test Bench with AND_OR as UUT

Note: The *Spartan 3E Board User Guide*, the *Spartan 3E Board Schematic Diagram*, and the *ISE 8.2i Quick Start Tutorial* will be useful during this exercise. Download them from <http://emp.byui.edu/fisherr/Tools.htm> or from our Blackboard course page under *Software*, and *References*.

Objectives

After completing this lab, you will be able to:

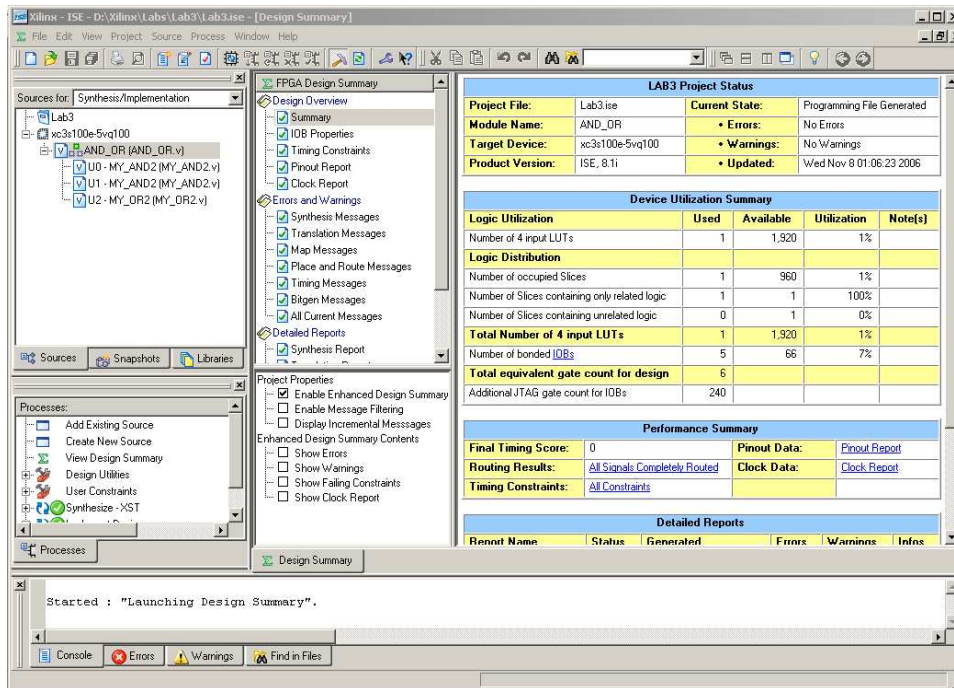
- Assign FPGA pins to input switches and output displays on the S3E FPGA board.
- Download a design into the S3E FPGA Board.
- Test an FPGA circuit for correct operation.

Procedure

1. Start the ISE Navigator. See the *ISE 8.2i Quick Start Tutorial*.
2. Open the previous project and update the FPGA information.

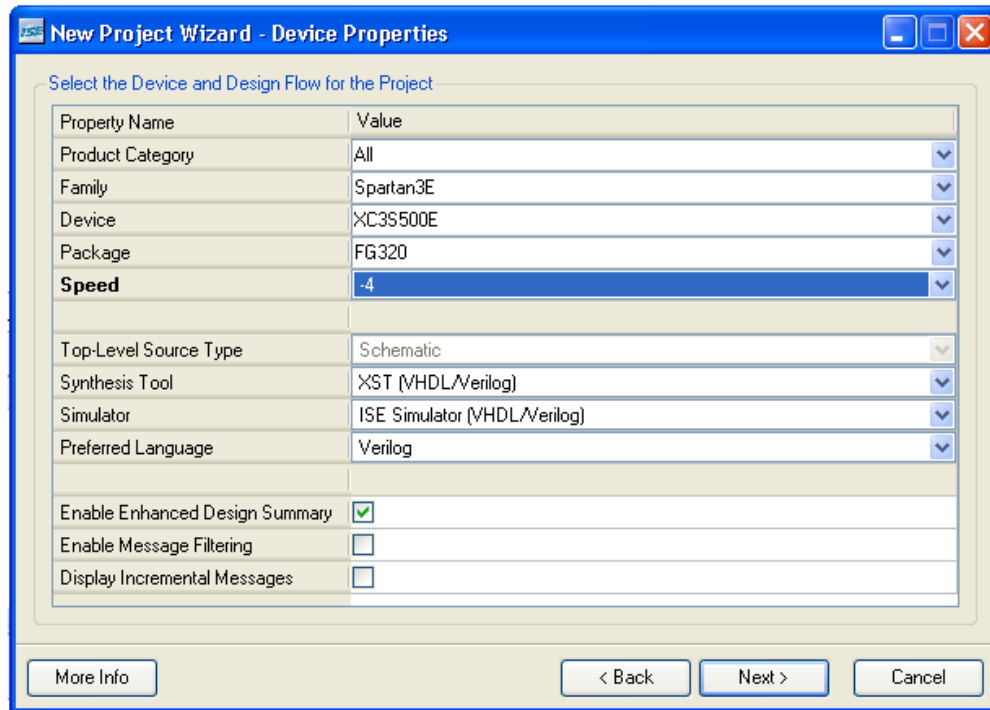
Select *File* → *Open Project*

Navigate to *C:\Xilinx\Labs\Lab3* and select *Lab3.isc*.



Double click on the FPGA in the *Sources* window.

Note: The window shown below reflects a newer version of the Xilinx software and device settings for the Spartan 3 Board currently used in the lab.



Enter the values shown above in the *Device Properties* box and click *OK*.

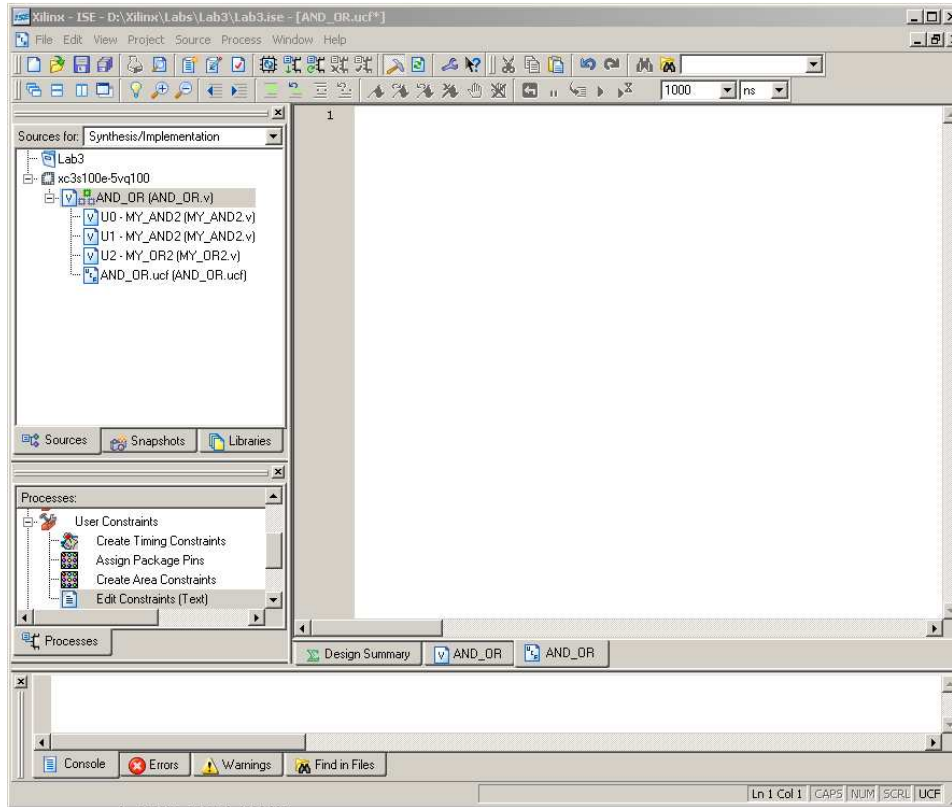
Click on the top level module (AND_OR.v).

3. Assign package pins.

Select AND_OR.v as the source file in the *Sources* window. Then expand *User Constraints* in the *Processes* window.

Double click *Constraints (Text)*.

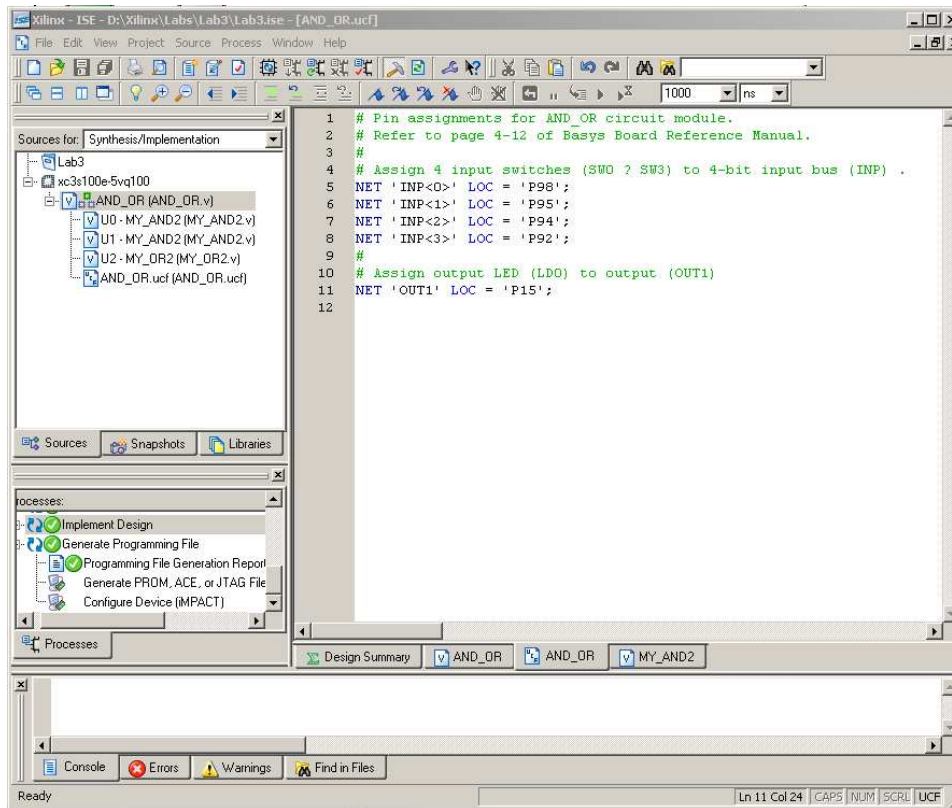
A dialog box will open that asks to add an Implementation Constraint File (UCF) to the project. Click *Yes*. An editing window will appear.



Type the following code, starting with line 1, as shown in the figure below.

```
# Pin assignments for AND_OR circuit module.
# Refer to pages 16 and 20 of the S3E User Guide.
#
# Assign 4 input switches (SW0 – SW3) to 4-bit input bus (INP) .
NET 'INP<0>' LOC = 'L13';
NET 'INP<1>' LOC = 'L14';
NET 'INP<2>' LOC = 'H18';
NET 'INP<3>' LOC = 'N17';
#
# Assign output LED (LD0) to output (OUT1)
NET 'OUT1' LOC = 'F12';
```

NOTE: Enter the code shown above. The code shown in the screen shot below is for an older version of the FPGA. The location names (LOC) show in the screen shot will NOT work with the S3E FPGA Board!



Save the Implementation Constraint File (UCF).

4. Download the circuit into the FPGA and test its operation.

Make sure the JTAG3 cable and the power supply are connected to the S3E FPGA Board.

Move the jumper on JP2 from the ROM position to the JTAG position. This will cause the FPGA to be programmed from the cable instead of reading the default program from the on-board ROM.

Double click on *Implement Design* in the *Processes* window. If there are no problems, a green check mark will replace the orange question mark.

Expand the *Generate Programming File* menu in the *Processes* window and double click *Configure Device (iMPACT)*. Wait for the new (iMPACT) window) to appear.

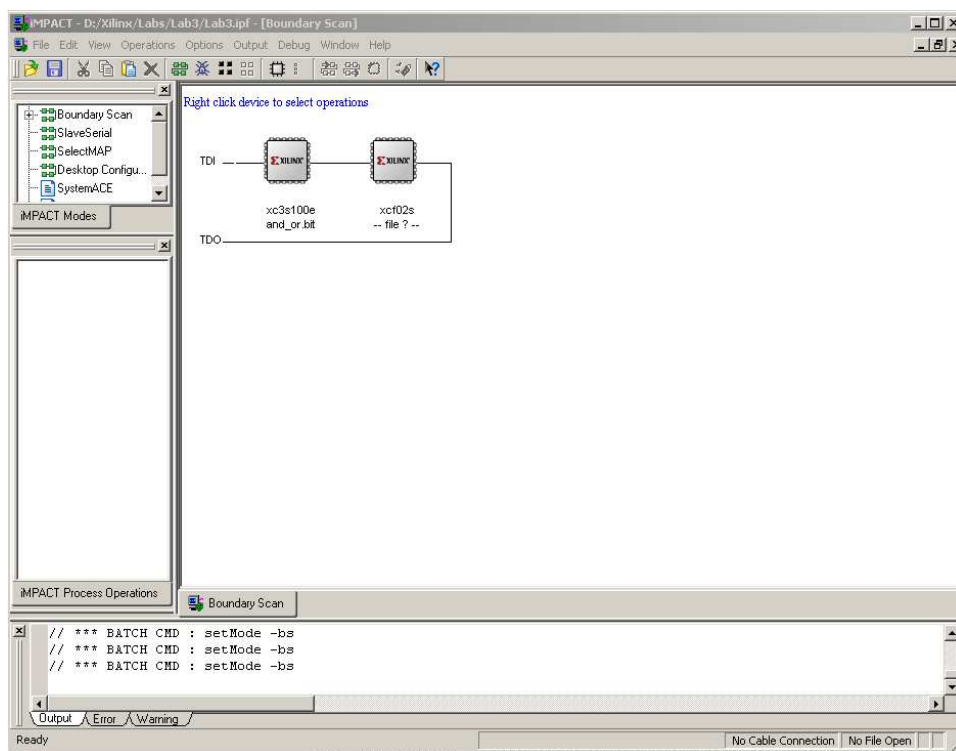
Select *Configure devices using Boundary scan (JTAG)* with the default option (*Automatically connect to a cable and identify Boundary-Scan chain*).

After the identification process is complete, a small window called *Assign a New Configuration File* will appear. Select *and_or.bit* (or other *.bit file if

you have named is differently). This is the file that will be programmed into the XC3S100E FPGA.

The same window will again appear. This time it is asking for the file to be programmed into the XCF02 Platform Flash ROM. Do not program the ROM. Select *Bypass* instead.

IMPORTANT: Why should you select *Bypass*? If you, instead, assign any file to this ROM, the default program & FPGA configuration will be erased. According to the ECE Department at the University of Minnesota, irreparable damage to your board will occur if your program has any errors. Do you want to risk it?



Right click on the *xc3s100e* device and select *Program*. Click *OK* to accept the default values in the *Programming Properties* window.

If all goes well, you will receive a message that states, "Programming Succeeded."

You may now remove the JTAG cable and test the hardware using the four input switches and the output LED.

NOTE: The bit stream you downloaded is volatile, which means that the FPGA is erased every time power is removed.